Cybersecurity – EC521
Memory Corruption

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Outline

Assembly Review

Vulnerabilities I

Vulnerabilities II

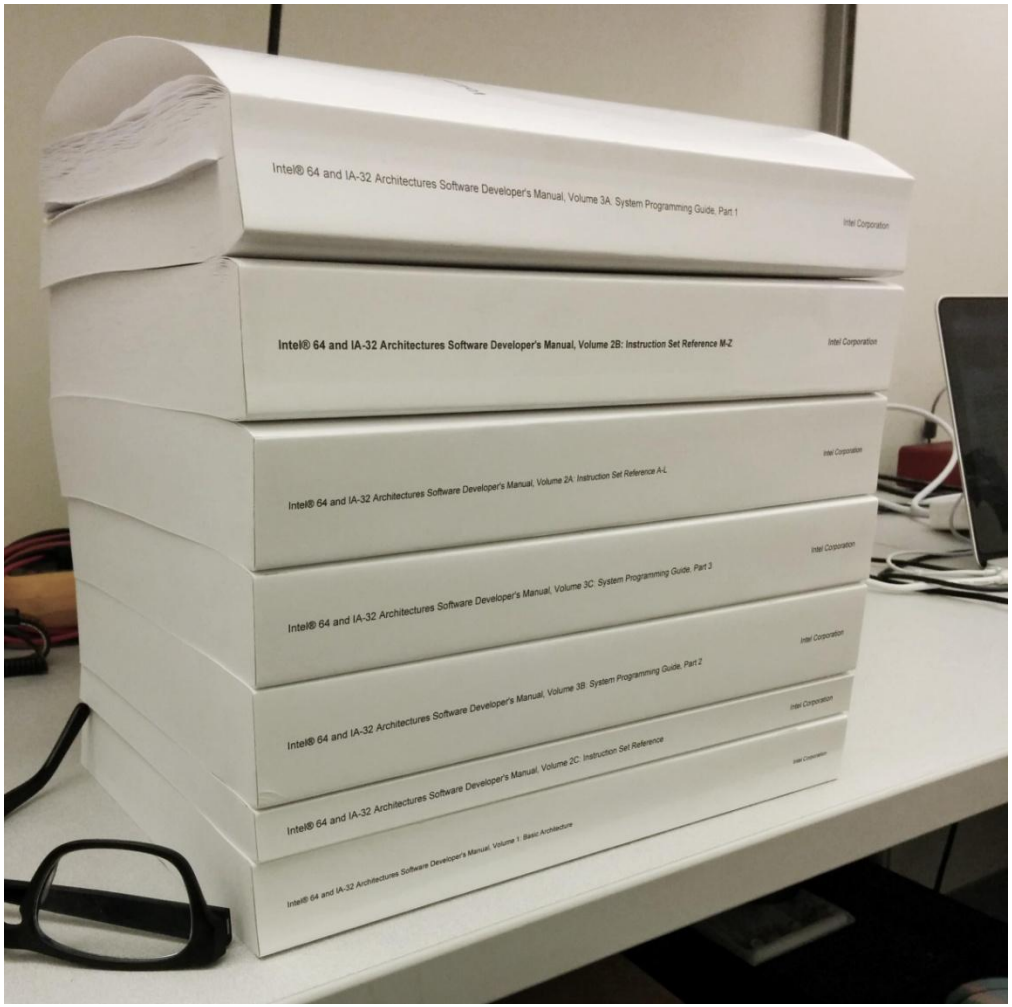
Defenses & Evasion of Defenses

Malware Analysis

Assembly Review

1. Correspondence between a (relatively) high-level language (C) and assembly
2. System components
   - CPU
   - Memory
3. Instructions
   - Formats
   - Classes
   - Control flow
4. Procedures

A Deep Topic


Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 3A: System Programming Guide, Part 1
Intel Corporation
Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 2B: Instruction Set Reference M-Z
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Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 2C: Instruction Set Reference
Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 1: Basic Architecture

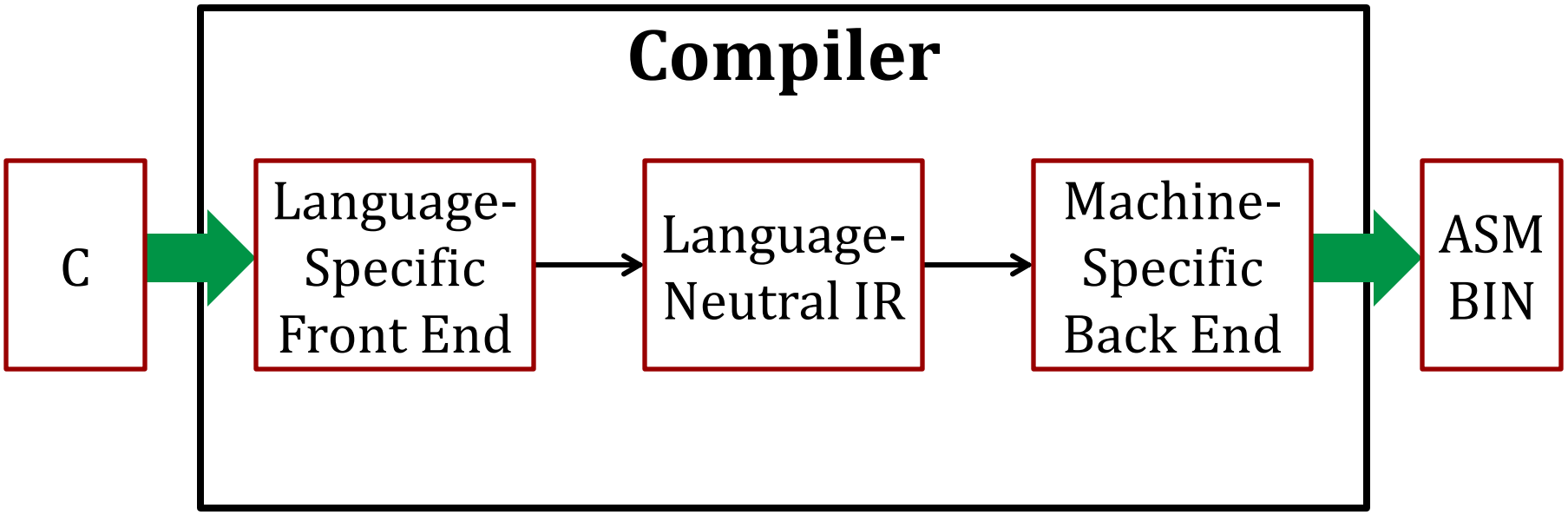
Compilers

```
int abs(int x) {
  if (x < 0)
    return -x;
  return x;
}
```

Computers don't execute source code (doh!)

- Instead, they operate on machine code
- *Compilers* translate code from a higher level to a lower level
- Today: C → assembly → machine code

Compilers


Compiler
C
Language-Specific Front End
Language-Neutral IR
Machine-Specific Back End
ASM BIN

Assembly

Human-readable machine code

- Simple translation to machine code

We will focus on x86/x86_64

- (Externally) CISC architecture
- Instructions have side effects

Assembly syntaxes

- Intel: `<mnemonic> <dst>, <src>`
- AT&T: `<mnemoic> <src>, <dst>`
- Examples will be in Intel syntax

Compilers

```
int abs(int x) {
  if (x < 0)
    return -x;
  return x;
}
```

C → ***assembly*** → machine code

Compilation (–O0 vs. –O3)

```
abs:
    pushrbp
    mov rbp, rsp
    mov dword ptr [rbp - 8], edi
    cmp dword ptr [rbp - 8], 0
    jge .LBB0_2

    mov eax, 0
    sub eax, dword ptr [rbp - 8]
    mov dword ptr [rbp - 4], eax
    jmp .LBB0_3
.LBB0_2:
    mov eax, dword ptr [rbp - 8]
    mov dword ptr [rbp - 4], eax
.LBB0_3:
    mov eax, dword ptr [rbp - 4]
    pop rbp
    ret
```

```
abs:
    mov  eax, edi
    neg  eax
    cmovl  eax, edi
    ret
```

Modern compilers are relatively sophisticated

CPU and Memory

Von Neumann Architecture

- Co-mingled code and data in memory
- Shared bus for code and data

CPU has program counter, points to (next) instruction

- Execution through repeated instruction cycles (fetch -- decode -- execute)
- Usually pipelined in modern architectures

Instruction set architectures (ISAs) have operational semantics

- Given an input state (registers, memory), will produce a well-defined output state

CPU and Memory

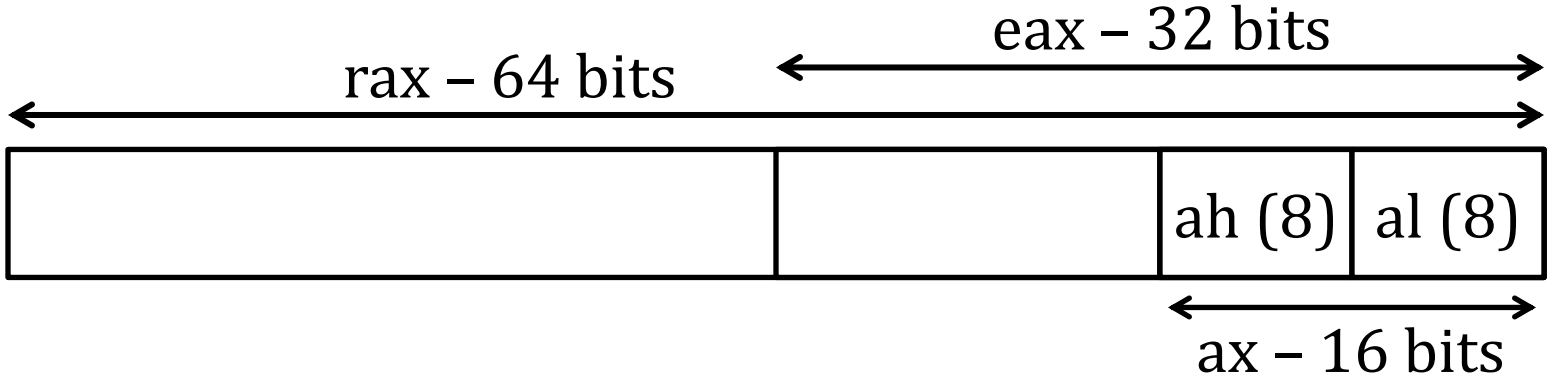
CPU contains registers

- Program counter (rip)
- Stack pointer (rsp)
- Frame pointer (rbp)
- General purpose registers
  - rax, rbx, rcx, rdx, rsi, rdi, r8-r15
- Contition codes (RFLAGS)
  - Affected by arthmetic and logical operations

Memory stores code and data

- Byte-addressable array

Registers



Convention:

- **`rax`** Accumulator
- **`rbx`** Pointer to data
- **`rcx`** Loop counter
- **`rdx`** I/O operations
- **`rdi`** Destination pointer (loops)
- **`rsi`** Source pointer (loops)

Flags

OF Overflow flag
DF Direction flag (loops)
SF Sign flag
ZF Zero flag
PF Parity flag
CF Carry flag

Bit vector of flags (RFLAGS)

- Automatically set and tested by instructions
- Many other fields

Executable File Format

Most common on Linux is ELF (man 5 elf)

- PE on Windows

Header

- Type (executable, library), architecture, offset of segment and section headers, etc.

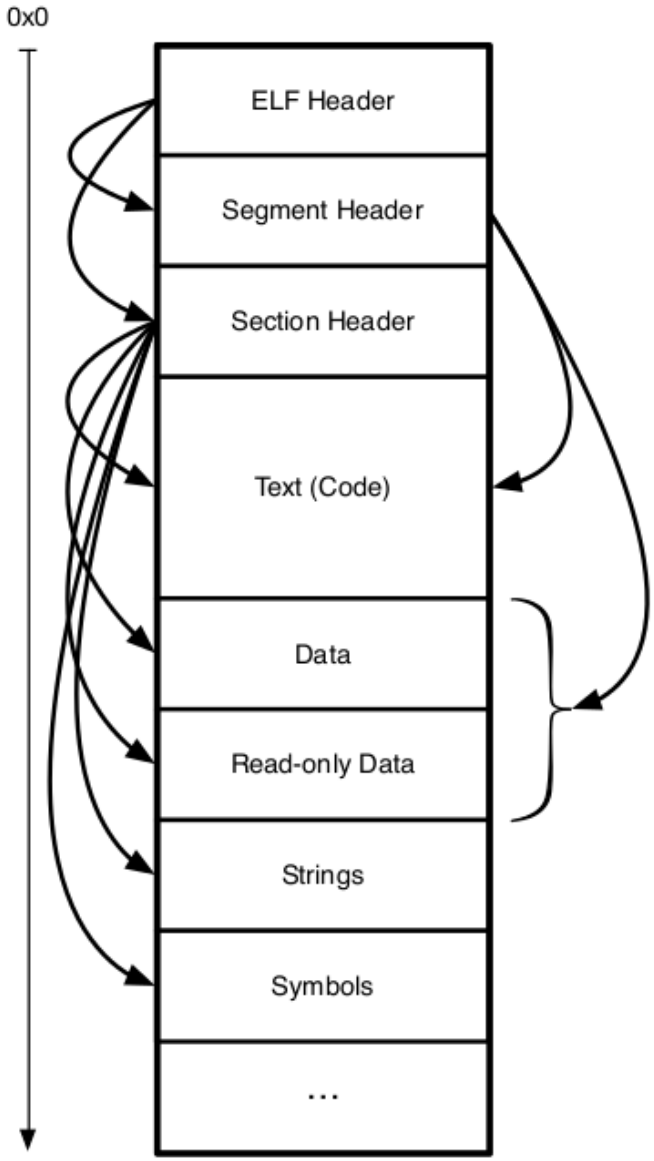
Segments

- Chunk of code, data necessary for execution
- Offset, size, type, virtual address

Sections

- Code, data, relocation info, symbols, debug info, etc.
- Offset, size, type

Structure of an ELF File



Memory Layout

Runtime loader is responsible for loading (usually) multiple binary objects into virtual memory

- Executable
- Libraries

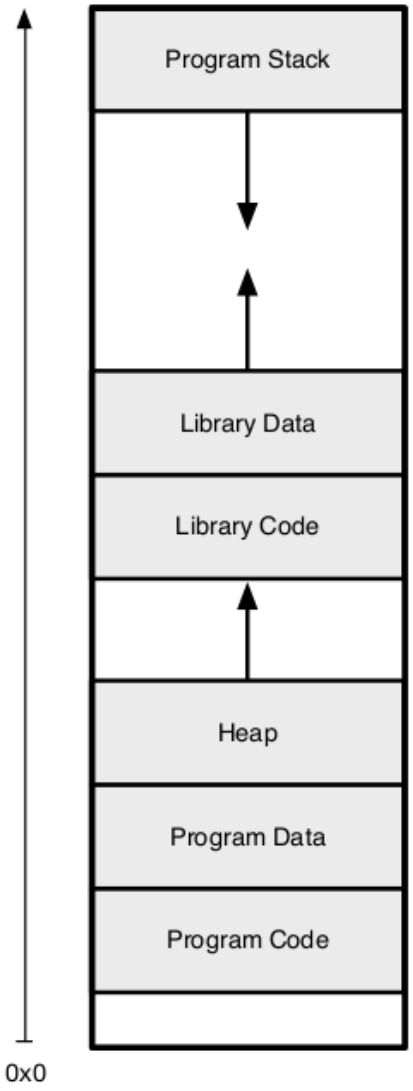
Heap

- Data segment for dynamic data
- Grows upwards, limit controlled by brk()

Stack

- Data segment for procedure-local data, control information
- Grows downwards (on the x86 family)

Memory Layout



Instruction Components

Mnemonic	Operands
nop	empty
neg	rax
add	rax, 0x10
mov	rax, rdx
mov	rax, byte[rdx]
mov	rax, dword[rdx+rcx*4]
jmp	0x08042860
jmp	[rdi]

Operand Types

Literal

- Integer constant directly encoded into the instruction
- e.g., `mov rax, 0x0` (constant 0 moved into rax)

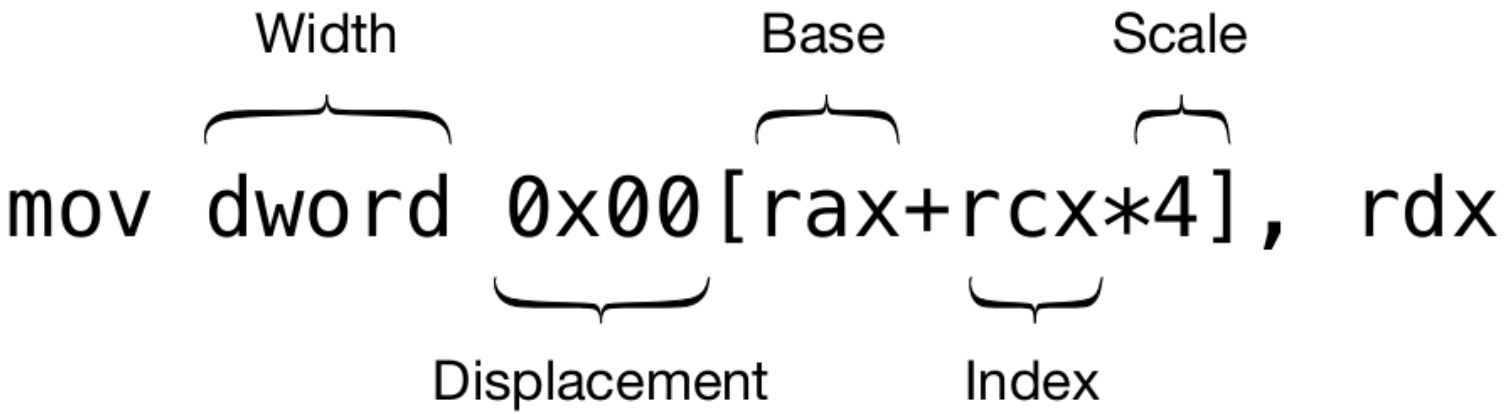
Register

- Contents of a named register
- e.g., `mov rax, rdx` (rdx is moved into rax)

Memory

- Memory reference
- e.g., `mov rax, dword [rdx]`

Memory References



Base Base of reference, register

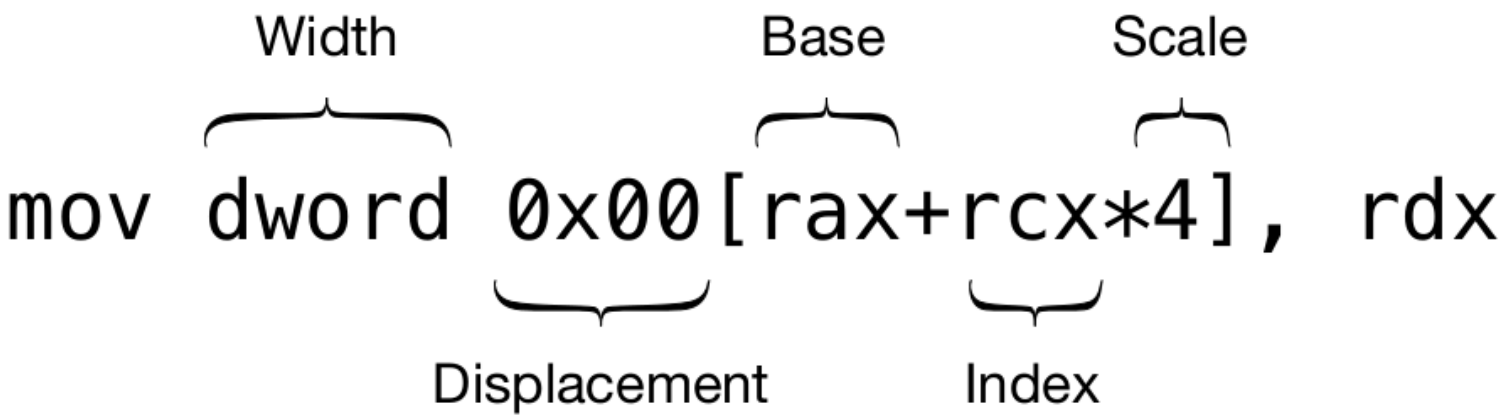
Index Offset from base

Scale Constant that scales index from base

Disp. Base of reference, constant

Width Scales reference

Common Widths



byte Obvious

word 16 bits

dword 32 bits (double word)

qword 64 bits (quad word)

Memory References

For example, this C snippet

```
int data[8]
…
data[1] = 4;
```

might translate to

```
lea rax, [rbp-0x40]
mov rdx, 0x04
mov rcx, 0x01
mov dword [rax + rcx * 4], rdx
```

Instruction Classes

Instructions grouped into different classes

- Load/store
- Arithmetic
- Logic
- Comparison
- Control transfer

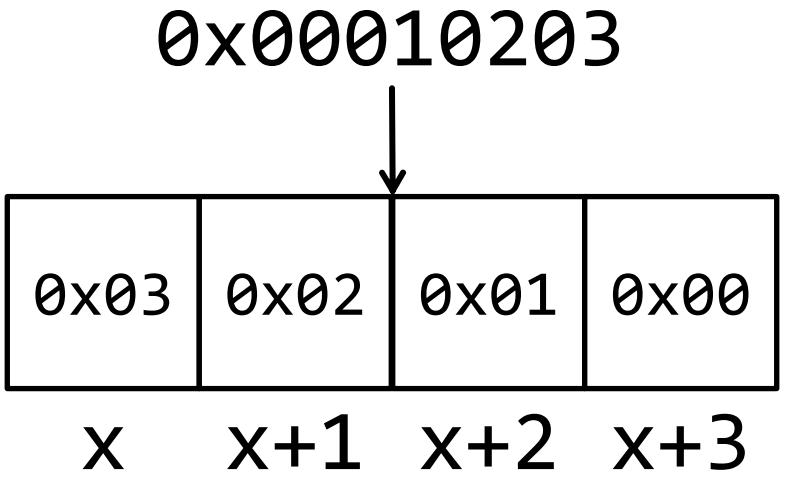
We'll go through a few common examples for each

- Impossible to cover everything here
- Compile programs, disassemble the output or capture assembly, and investigate *yourself*!
- RTFM! (read the ***fine*** manual)

Common Loads, Stores

Instruction	Effect	Description
`mov y, x`	y ← x	Move x to y
`movsx y, x`	y ← SignEx(x)	Move sign-extended x to y
`movzx y, x`	y ← ZeroEx(x)	Move zero-extended x to y
`push x`	rsp ← rsp – 8	Decrement rsp by 8
	Mem(rsp) ← x	Store x on stack
`pop x`	x ← Mem(rsp)	Load top of stack in x
	rsp ← rsp + 8	Increment rsp by 8
`lea y, x`	y ← Addr(x)	Store address of x to y

Endian-ness



The x86 family is a little-endian architecture

- Multi-byte values stored least-significant byte first

If you have a `uint8_t*` pointer to address x

- What is the value for x[0]? x[3]?

Types and the Lack Thereof

Memory at this level: Just a chunk of bytes

- No primitive types, structs

Data can have multiple interpretations

- Signed or unsigned?
- Store a 32-bit value, read back a 16-bit value
- Overlapping loads, stores

Common Arithmetic

Instruction	Effect	Description
`add y, x`	$y \leftarrow y + x$	Add x to y
`sub y, x`	$y \leftarrow y - x$	Subtract x from y
`mul x`	$y \leftarrow rax \times x$	Signed multiply of rax and x
	$rdx \leftarrow High(r)$	High bits stored in rdx
	$rax \leftarrow Low(r)$	Low bits stored in rax
`div x`	$r \leftarrow \frac{rdx:rax}{x}$	Divides rdx:rax by x
	$rdx \leftarrow Rem(r)$	Remainder stored in rdx
	$rax \leftarrow Quo(r)$	Quotient stored in rax

Common Logic

Instruction	Effect	Description
`and y, x`	$y \leftarrow y \wedge x$	Logical AND stored in y
`or y, x`	$y \leftarrow y \vee x$	Logical OR stored in y
`xor y, x`	$y \leftarrow x \oplus y$	Logical XOR stored in y
`shl y, x`	y ← ShiftLeft(y, x)	Shift y left by x bits
`shr y, x`	y ← ShiftRight(y,x)	Shift y right by x bits
`sal x`	y ← SShiftLeft(y,x)	Signed left shift
`rol y, x`	y ← RotateLeft(y,x)	Rotates y left by x bits

Comparison

Instruction	Effect	Description
`test y, x`	$t \leftarrow y \wedge x$	Performs logical AND
	$SF \leftarrow MSB(t)$	Sets SF if MSB set in result
	$ZF \leftarrow t \stackrel{?}{=} 0$	Sets ZF if result is 0
	…	
`cmp y, x`	$t \leftarrow y - x$	Performs signed subtraction
	$SF \leftarrow MSB(t)$	Sets SF if MSB set in result
	$ZF \leftarrow t \stackrel{?}{=} 0$	Sets ZF if result is 0
	…	

Control Transfers

Control transfers change control flow of programs

- Can be predicated on results of a previous comparison (flag bits)
- Arithmetic, logic instructions also set flags (omitted before for brevity)

Distinction between *jumps* and *calls*

- Jumps simply transfer control with no side effects
- Calls used to implement procedures

Distinction between *direct* and *indirect* transfers (*indirect* also known as computed transfers)

- Direct transfers use relative offsets, indirect transfers are absolute (through a register or memory reference)